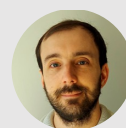
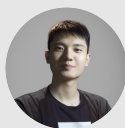
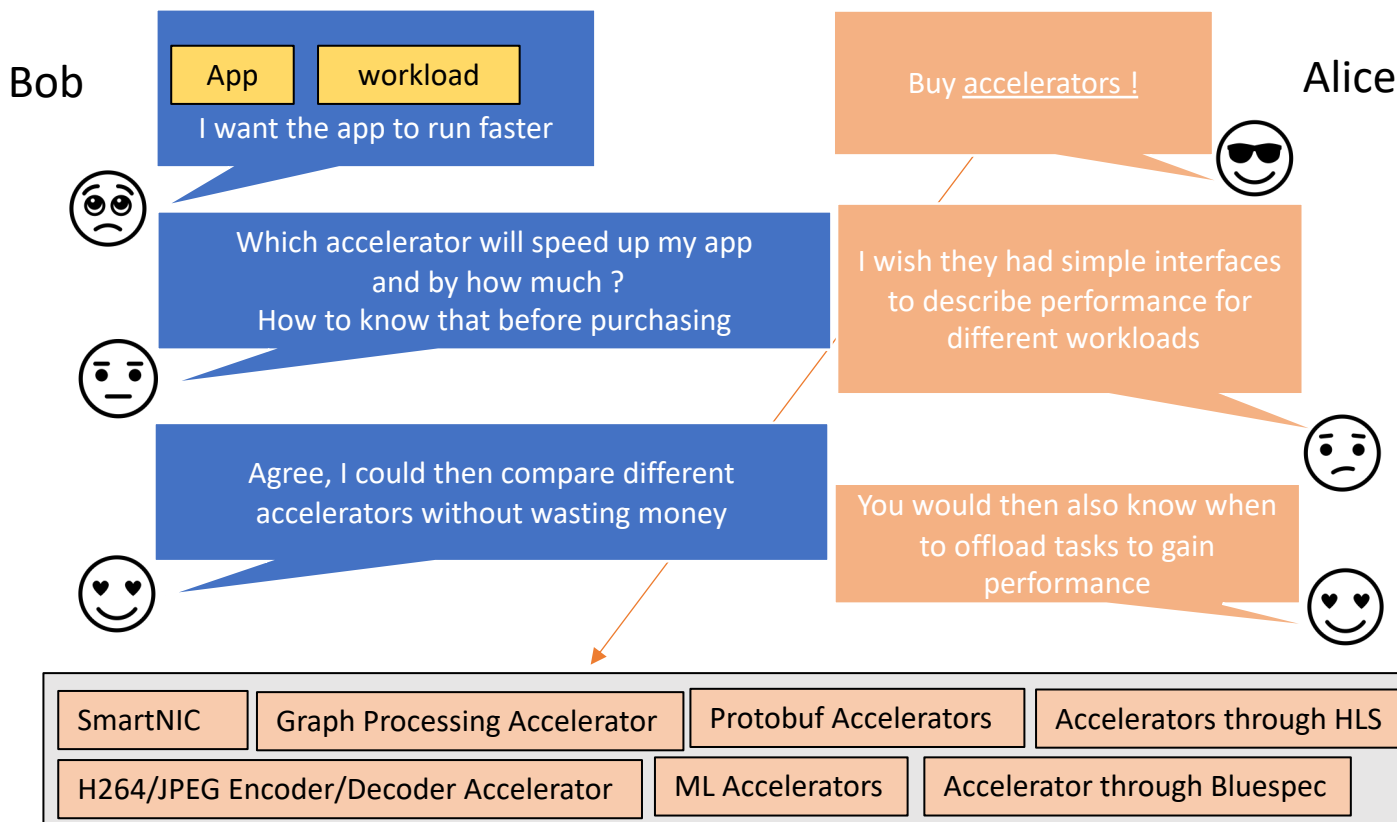


Performance Interfaces for Hardware Accelerators

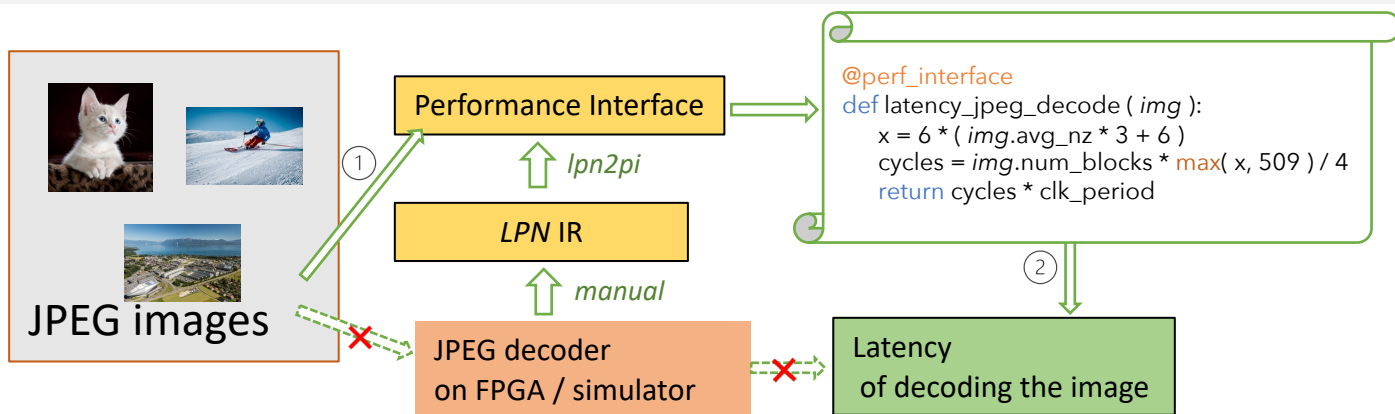


Jiacheng Ma, Rishabh Iyer, Mahyar Emami, Sahand Kashani, Thomas Bourgeat, George Candea

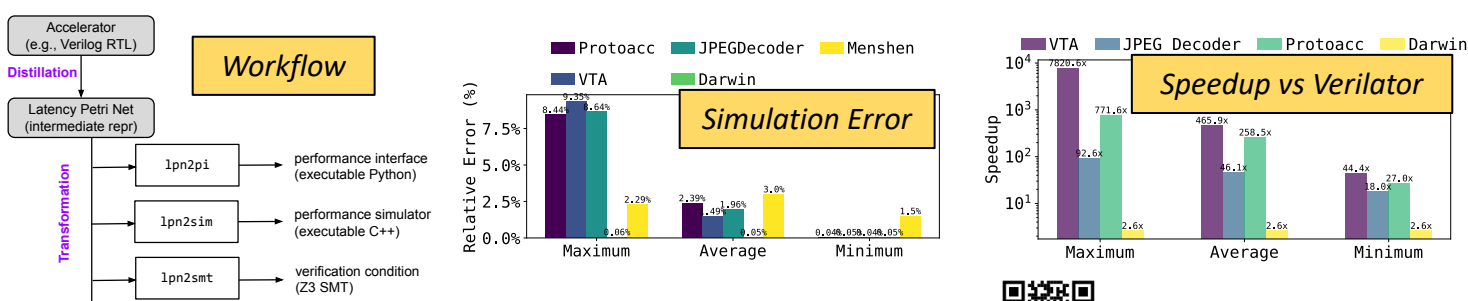
Reality: People want to use accelerators, but ...



Goal: Human understandable interfaces for accelerators' performance! (The only alternative to know performance now is profiling)



LPN (Latency Petri Nets) is formal, analyzable, accurate and fast to simulate



Want to know more? Talk to us

