IIBLAST: Speeding Up Commercial FPGA Routing by Decoupling and Mitigating the Intra-CLB Bottleneck

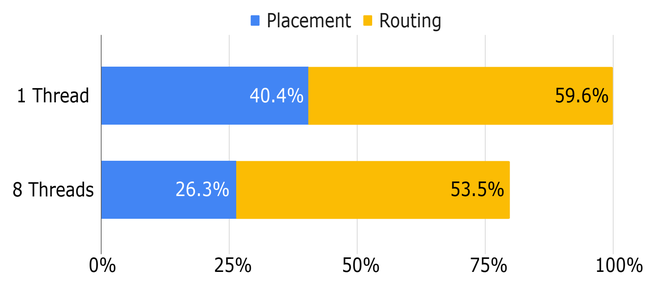
Shashwat Shrivastava, Stefan Nikolić, Chirag Ravishankar‡, Dinesh Gaitonde‡, and Mirjana Stojilović

EPFL ‡AMD

SCAN FOR ARTIFACTS

Routing vs Placement Runtime

1

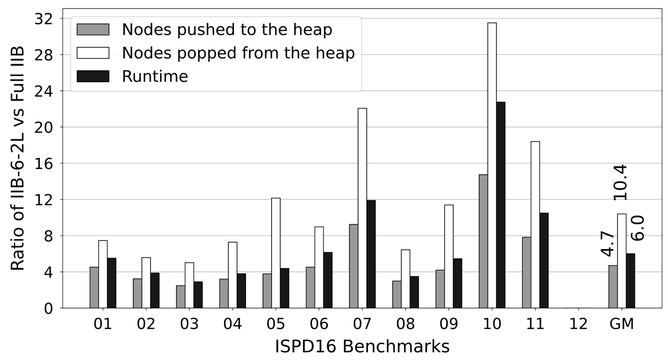


Routing is the major compilation bottleneck

Impact of Commercial IIB

2

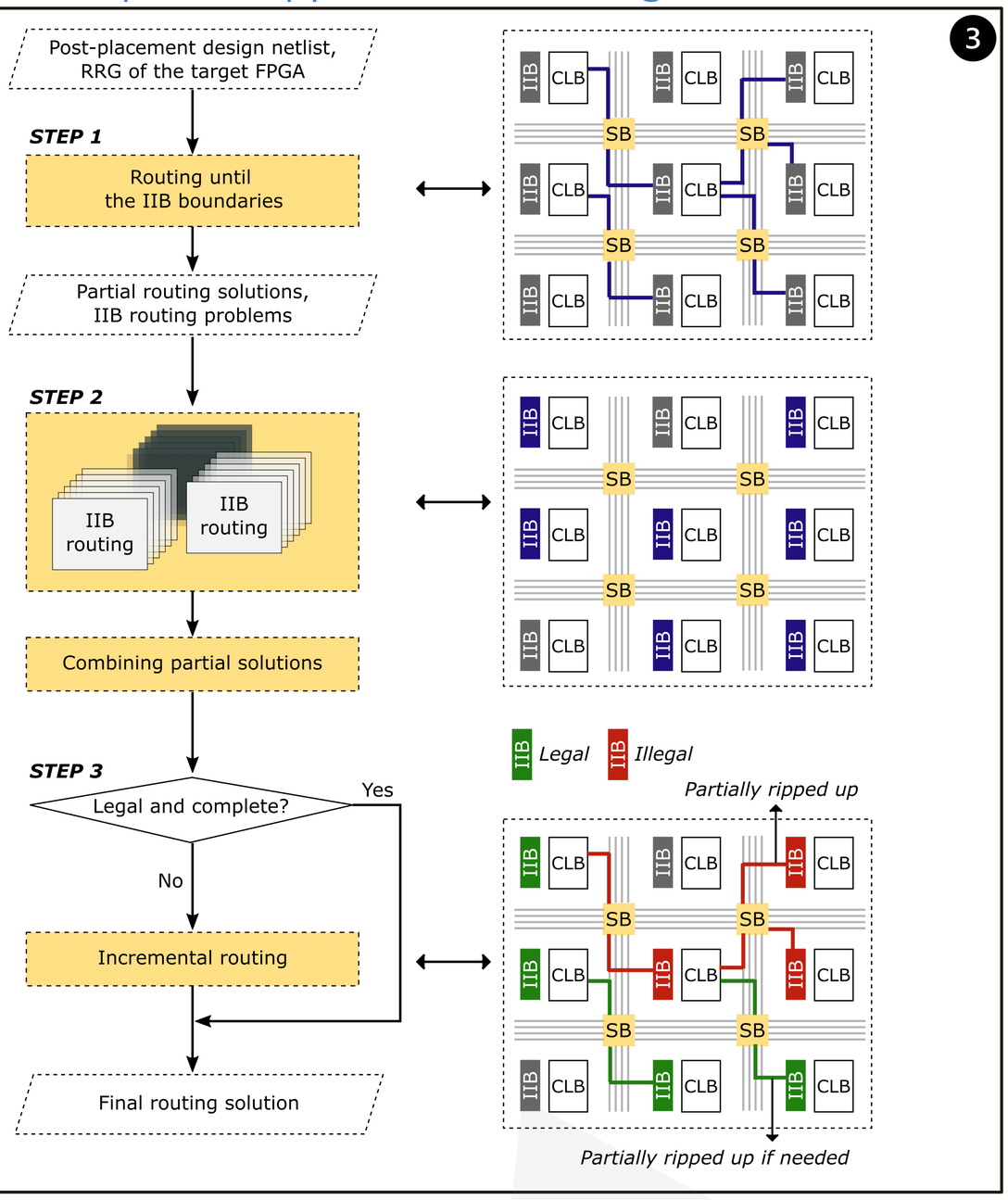
Routing through a commercial IIB closely resembling an AMD UltraScale FPGA (IIB-6-2L, two layers of 6:1 mux) vs a fully connected IIB (Full IIB)



Routing through commercial IIB is 6× slower

Proposed Approach: Multi-Stage Router

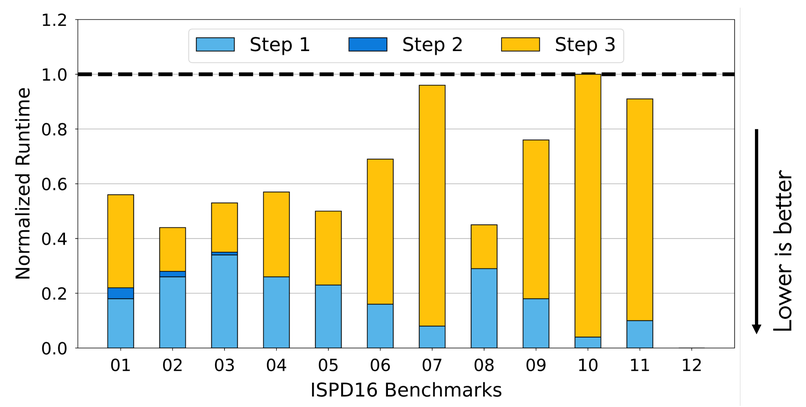
3



Multi-Stage Router vs Single-Stage Router

4

Geomean runtime improvement 1.5×

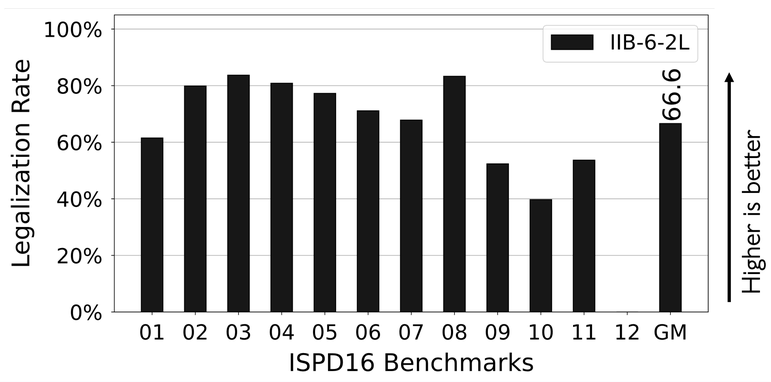


Step 3 consumes significant fraction of runtime

What is Increasing Step 3 Runtime?

5

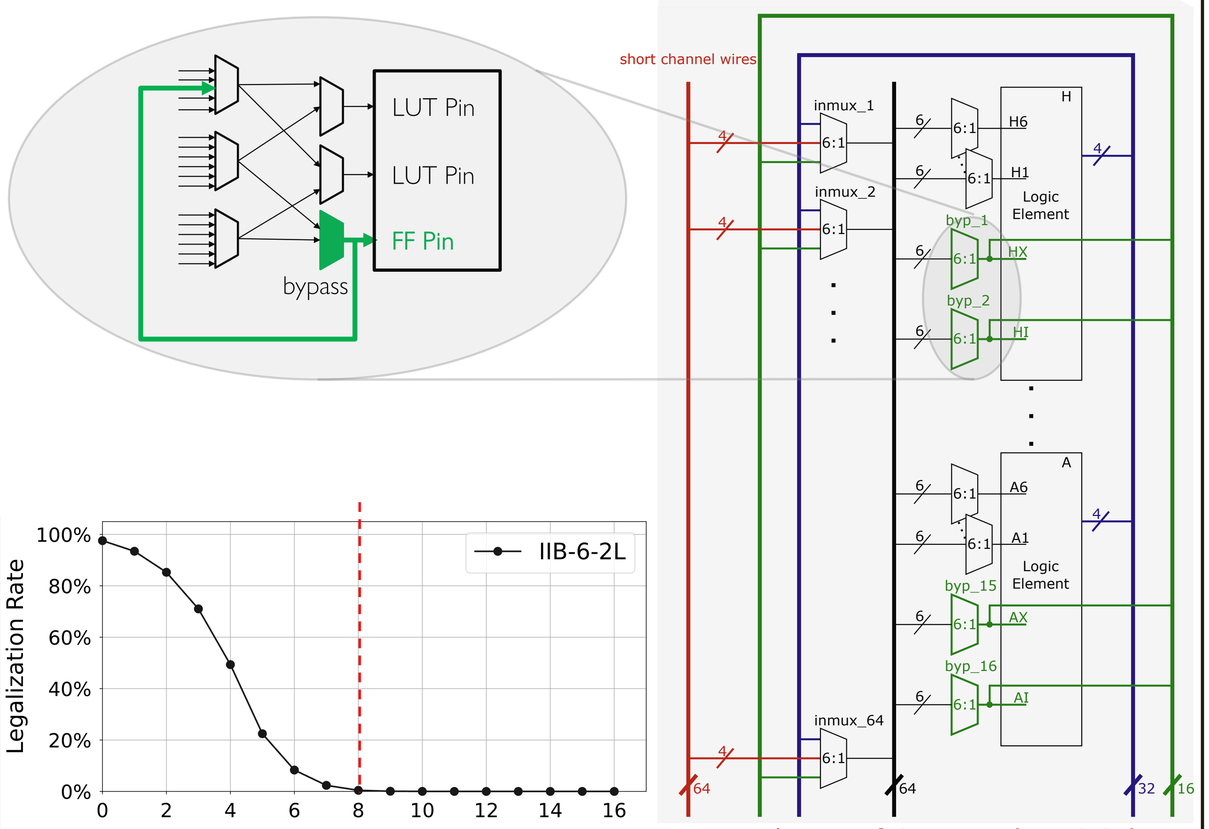
Only 66% of IIBs legalize in Step 2, on average



Low legalization rate increases runtime of step 3

Reason for Low Legalization Rate

6



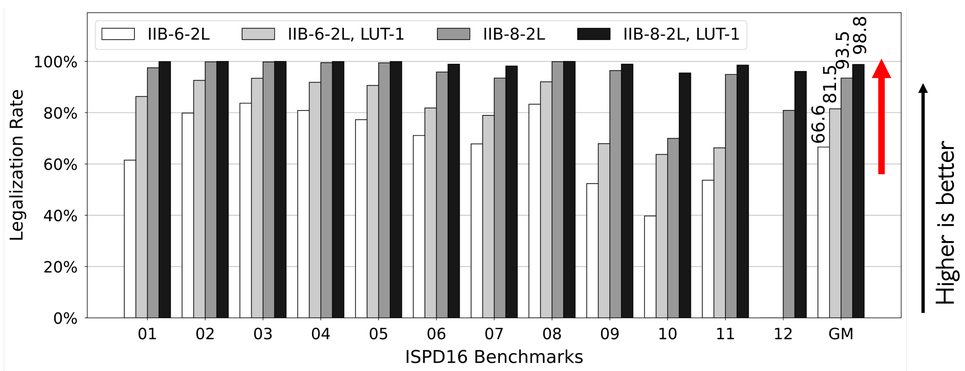
Legalization rate drops to zero if ≥ 8 bypass pins are used

Multi-Stage Router with Enhancements

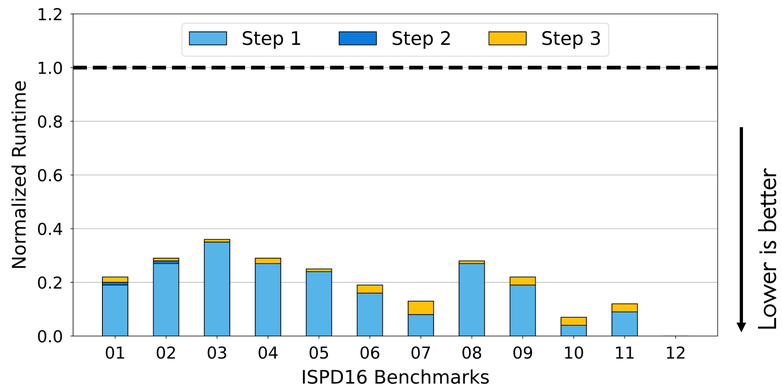
7

Techniques to increase legalization rate:

- Route a net driving a FF through a free LUT → LUT-1
- Increase IIB mux size from 6:1 to 8:1 → IIB-8-2L



Geomean runtime improvement 5×



Recovered the runtime improvement from 1.5× to 5×

Our Multi-Stage Router coupled with architectural enhancements reduces runtime by 5×