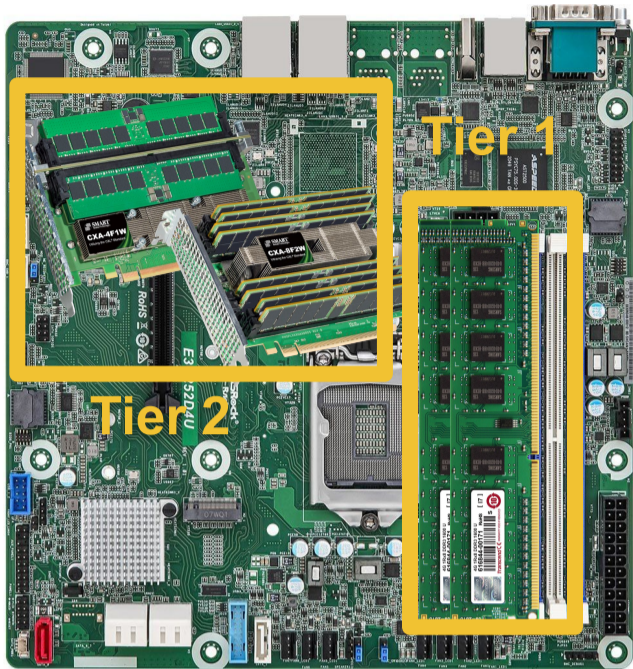


# Handling Latency in Tiered Memory with Prefetching

Musa Unal, Vishal Gupta, Yueyang Pan, Yujie Ren, Sanidhya Kashyap

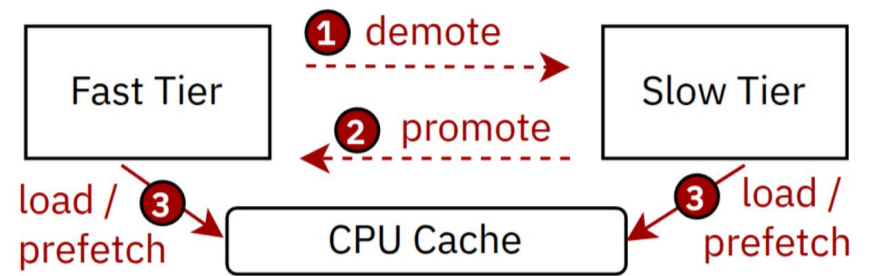
**Problem:** Tiering systems do not consider how application is accessing the data



Data centers use different types of memories which have different characteristics.

Trade-off between

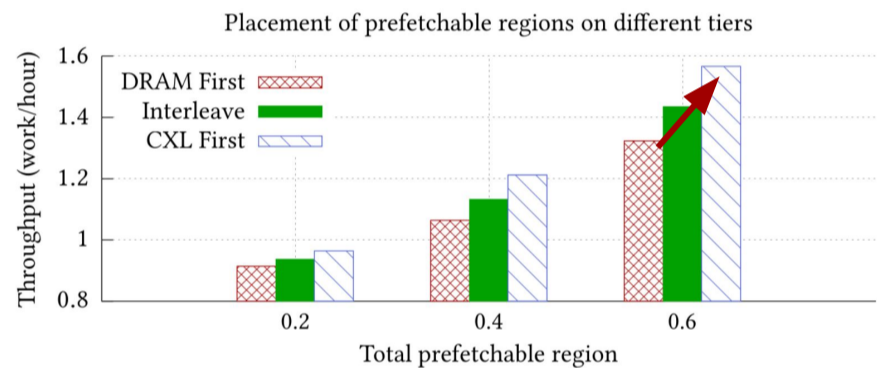
- Latency/Bandwidth
- Price
- Energy



Current tiering systems are trying to optimize load time (3) by demoting (1) and promoting (2) between the nodes.

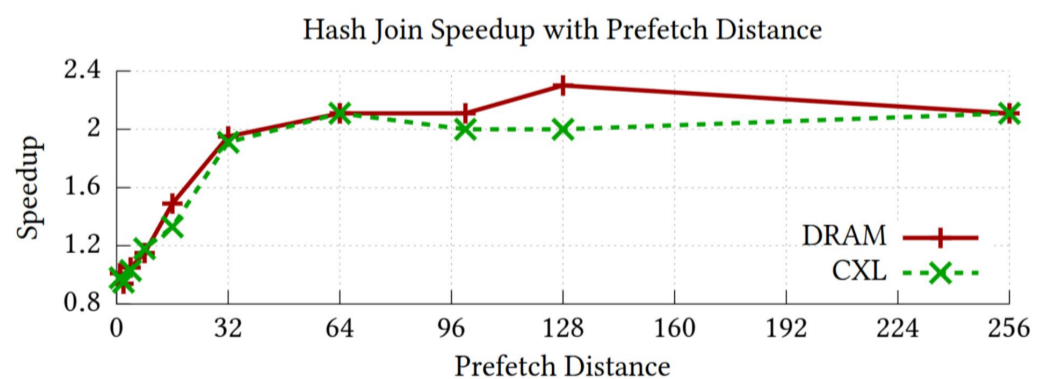
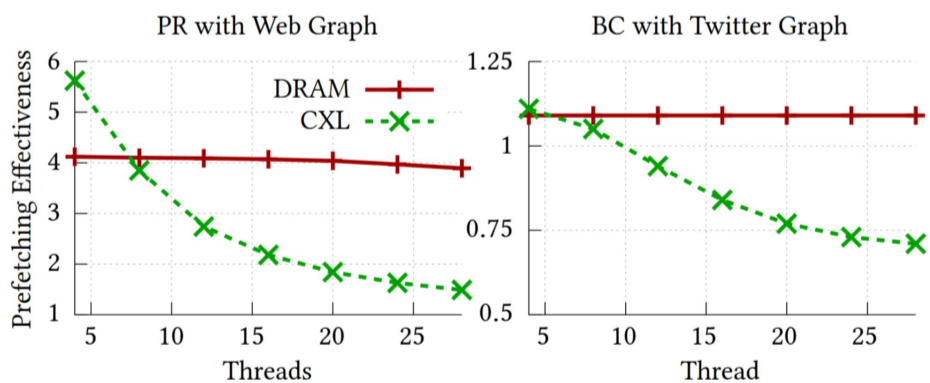
**Insight:** Data prefetchers can tolerate CXL latency.

Hardware prefetchers and software prefetching can **hide** the CXL latency

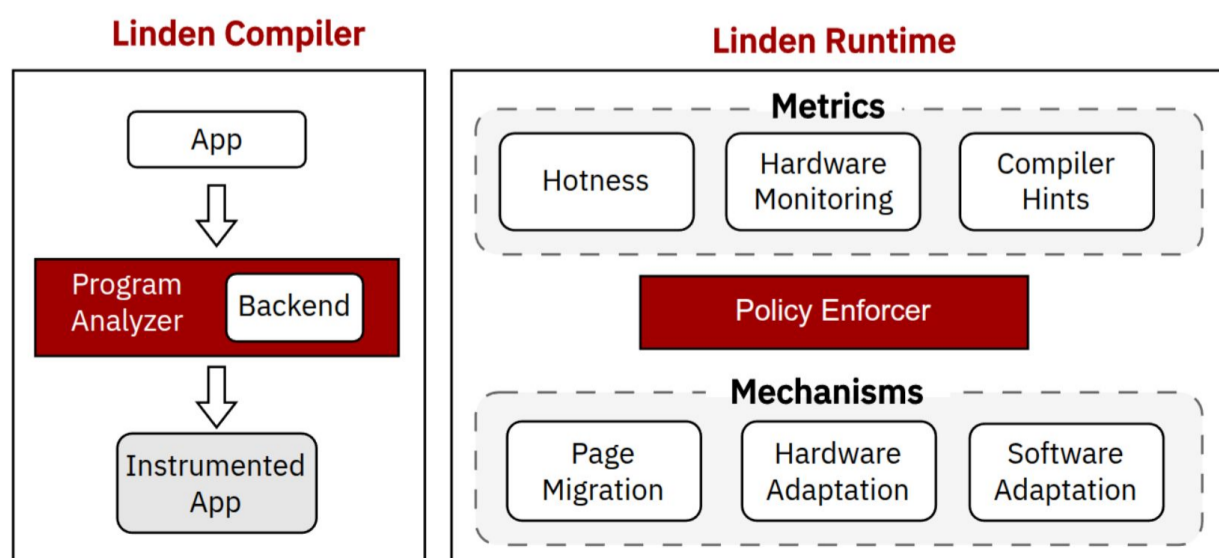


**Hardware prefetchers** can degrade performance under high load.

**Software prefetches** must use tiering-aware prefetch distances to be effective.



**Proposal:** A runtime system to effectively use prefetchers on tiered memory



**Reduce:** Minimize latency by increasing the locality.  
**Tolerate:** Hide the latency by prefetching.

1. Detect prefetchable regions
2. Monitor memory bandwidth
3. Enforce different policies regarding to application's needs